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| EXAMINER | |
|---|---|
| HSIEH, HSIN YI | |

| ART UNIT | PAPER NUMBER |
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| 2811 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/580,625 | HUETING ET AL. | |
| | Examiner | Art Unit | |
| | Hsin-Yi (Steven) Hsieh | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claim 11 is objected to because of the following informalities: Claim 11 recites 'the gate" in the last line. Changing this limitation to "the conductive gate electrode" is suggested.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 15-18** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. The term "steeply" in claim 15 is a relative term which renders the claim indefinite. The term "steeply" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Claim 15 recites "steeply" in the 20$^{th}$ line of the claim, which is only disclosed in 4$^{th}$ paragraph of page 3 and is not defined.

5. Claims 16-18 are rejected because they depend on the rejected claim 15.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claim 15** is rejected under 35 U.S.C. 102(b) as being anticipated by Omura et al. (EP 1168455 A2) as can be understood since claims 15-18 have been rejected under 35 U.S.C. 112.

8. Regarding **claim 15**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11) past the source region (14) and the body region (13) into the drift region (12), each

insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode(19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and wherein the drift region (12) has a steeply graded doping concentration (see Fig. 15B, the change of doping concentration of Fig. 15B is considered as "steeply") that increases from the part of the drift region (12) adjacent to the body region (13) to the part of the drift region (12) adjacent to the drain region (11; see Fig. 15B).

### *Claim Rejections - 35 USC § 103*

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. **Claims 1, 4-7, 9-10, and 12-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. (EP 1168455 A2).

12. Regarding **claim 1**, Omura et al. teach an insulated gate field effect transistor (power semiconductor switching element; [0001]), comprising: a semiconductor body (11, 12, 13 and 14; Fig. 2, paragraph [0023]) having opposed first and second major surfaces (the top surface of 13 and the bottom surface of 11; Fig. 2); a source region (source layer 14; Fig. 2, paragraph [0023]) of a first conductivity type (n-type; paragraph [0023]) at the first major surface (the top surface of 13); a body region (well layer 13; Fig. 2, paragraph [0023]) of a second conductivity type (p-type) opposite to the first conductivity type (n-type) under the source region (14; see Fig. 2); a drift region (drift layer 12; Fig. 2, paragraph [0023]) of the first conductivity type (n-type; paragraph [0023]) under the body region (13; see Fig. 2); a drain region (semiconductor substrate 11; Fig. 2, paragraph [0023]) of the first conductivity type (n-type) under the drift region (12; see Fig. 2), so that the source (14), body (13), drift (12) and drain regions (11) extend in that order from the first major surface (the top surface of 13) towards the second major surface (the bottom surface of 11); and insulated trenches (trench 15; Fig. 2, paragraph [0024]) extending from the first major surface (the top surface of 13) towards the second major surface (the bottom surface

of 11) past the source region (14) and the body region (13) into the drift region (12), each insulated trench (15) having sidewalls (see Fig. 2), and including insulator (first insulating film 16 and second insulating film 18; Fig. 2, paragraph [0024]) on the sidewalls (see Fig. 2), at least one conductive gate electrode (gate electrode 19; Fig. 2, paragraph [0024]) adjacent to the body region (13) separated from the body region (13) by a gate insulator (second insulating film 18; Fig. 2, paragraph [0024]), and at least one conductive field plate electrode (buried electrode 17; Fig. 2, paragraph [0024]) adjacent to the drift region (12) separated from the drift region (12) by a field plate insulator (first insulating film 16; Fig. 2, paragraph [0024]), and a gate-field plate insulator (18) separating the conductive field plate electrode (17) from the conductive gate electrode(19), wherein the source regions (14) and the insulated trenches (15) define a pattern of cells across the first major surface (stripped pattern; Fig. 1, paragraph [0022]); and the doping concentration in the drift region (12) increases from the part of the drift region (12) adjacent to the body region (13) to the part of the drift region (12) adjacent to the drain region (11; see Fig. 15B, paragraph [0053]),

Omura et al. do not teach the gate-field plate insulator (18) having a thickness that is greater than or equal to a thickness of the field plate insulator (16), and the doping concentration in the drift region (12) being at least 50 times greater adjacent to the drain region (11) than adjacent to the body region (13).

Parameters such as the thicknesses of the gate-field plate insulator and the filed plate insulator, and the doping concentration in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003] or the

breakdown voltage and the threshold voltage in paragraph [0065]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the thicknesses of the gate-field plate insulator and the filed plate insulator and the doping concentration within the range as claimed in order to achieve desired device performance.

13. Regarding **claim 4**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein a breakdown voltage of the insulated gate field effect transistor is less than or equal to 30V.

Omura et al. teach a device with a breakdown voltage of 50V (paragraph [0045]). Omura et al. also teach that the breakdown voltage and the ON resistance satisfy the inequality: $Ron < 2.2 \times 10^{-5} Vb^{2.25}$.

Parameters such as the breakdown voltage and the ON resistance in the art of semiconductor manufacturing process are the tradeoff between the device's performance and reliability and are subject to changes due to the requirement of the application, e.g. whether the performance (lower ON resistance) is more important than the reliability (higher break down voltage). Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to lower the breakdown voltage to less than or equal to 30V as claimed in order to achieve a lower ON resistance to improve device performance.

14. Regarding **claim 5**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the pattern of cells defined by the source regions (14) and the insulated trenches (15) arranged across the first major surface (the top surface of 13) is a pattern in which cells repeat in more than one direction across the surface to form a three-dimensional cell structure (see Fig. 25).

15. Regarding **claim 6**, Omura et al. also teach an insulated gate field effect transistor according to claim 5 wherein the cells are arranged in a hexagonal pattern (see Fig. 25)

16. Regarding **claim 7**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising an additional trench (the trench formed between the interlevel dielectric films 22; Fig. 4; paragraph [0026]) filled with conductive material (the conductive material of the source electrode 21; Fig. 4, paragraph [0026]) extending through the source region (14) to the body region (13) to connect a source contact (source electrode 21) to the source region (14) and the body region (13; see Fig. 4).

17. Regarding **claim 9**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the thickness of the insulator (16; Fig. 2) adjacent to the conductive field plate electrode (17) is greater than the thickness of the insulator (18) adjacent to the conductive gate electrode (19; see Fig. 2, paragraph [0031]).

18. Regarding **claim 10**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the cell pitch is not greater than 1 micron.

Parameters such as the cell pitch in the art of semiconductor manufacturing process are subject to change due to the requirement of the device performance. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to use a cell pitch not greater than 1 micron as claimed to achieve the required performance.

19. Regarding **claim 12**, Omura et al. do not teach an insulated gate field effect transistor according to claim 1 wherein the field plate insulator (16) has a thickness between 0.6 to 1 microns and the gate insulator (18) has a thickness between 0.2 to 0.5 microns.

Omura et al. teach that the thickness of the field plate oxide (16) is determined by the breakdown voltage and the thickness of the gate oxide (18) is determined by the threshold voltage (paragraph [0031]) Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to have the thickness of the field plate oxide and the thickness of the gate oxide as claimed as a result of achieving a desired or required breakdown voltage and threshold voltage.

20. Regarding **claim 13**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 wherein the conductive field plate electrode (17) is connected to the source region (21; Fig. 3, paragraph [0026])

21. Regarding **claim 14**, Omura et al. also teach an insulated gate field effect transistor according to claim 1 further comprising a field plate terminal connected to the conductive field plate electrode for controlling a field plate voltage independently (this is implied in the paragraph [0027], where Omura et al. disclose a voltage applied to each buried electrode 17, which obviously need a terminal connected to the buried electrode 17 to control the voltage).

22. **Claims 2 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 1 above, and further in view of Onda et al. ("SIC Integrated MOSFETs" Physica Status Solidi (A), Applied Research, Berlin, DE, vol. 162, no. 1, 16 July 1997, pages 369-388).

Omura et al. teach, regarding to **claim 11**, the first conductivity type is n-type (the conductivity type of the source region; paragraph [0023]), the second conductivity type is p-type (the conductivity type of the body region; paragraph [0023]).

Omura et al. do not teach, regarding to **claim 2**, the conductive gate electrode is of conductive semiconductor doped to be the second conductivity type (i.e. p-type), and regarding to **claim 11**, the gate is of p-type doped polysilicon.

In the same field of endeavor of semiconductor device, Onda et al. teach the gate electrode is a p-type doped polysilicon (Fig. 1, page 371 line 27). Onda et al. also teach that p-type polysilicon is used to form an accumulation mode SiC trench MOSFET (page 371, lines 23-43).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Onda et al. and use the gate taught by Onda et al., because an accumulation mode SiC trench MOSFET can be formed as taught by Onda et al.

23. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 1 above, and further in view of Miyano et al. (JP 403211885A).

Regarding **claim 3**, Omura et al. do not teach the conductive gate electrode has side pieces spaced apart adjacent to the sidewalls on either side of the insulated trench and a top piece spanning the gap between the side pieces.

In the same field of endeavor of semiconductor device, Miyano et al. teach the conductive gate electrode (gate electrode 3; Fig. 1, [Application example]) has side pieces (the left side and the right pieces with deeper depth) spaced apart adjacent to the sidewalls on either side of the insulated trench (a trench; Fig. 1 and 2, [Application example]) and a top piece spanning the gap between the side pieces (see Fig. 1 of the middle portion of gate electrode 3 with shallower depth than the left side and the right side pieces).

Miyano et al. also teach the shape of the gate reduces the capacitance between the gate and the drain, and a high speed operation can be performed ([Operation]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Miyano et al. and use the gate taught by Miyano et al., because the speed of the device can be improved as taught by Miyano et al.

24. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 7 above, and further in view of Hshieh et al. (US 2001/0003367 A1).

Regarding **claim 8**, Omura et al. do not teach a doped contact region of the second conductivity type in the body region in contact with the conductive material in the additional trench, the doping concentration in the doped contact region being higher than the doping in the rest of the body region.

In the same field of endeavor of vertical transistors, Hshieh et al. teach a doped contact region (P+ region 138; Fig. 2, paragraph [0025]) of the second conductivity type (p type) in the body region (in the P-body region; Fig. 2, paragraph [0025]) in contact with the conductive material (source metal layer 160; Fig. 2, paragraph [0025]) in the additional trench (source contact openings 150; Fig. 2, paragraph [0025]), the doping concentration in the doped contact region being higher than the doping in the rest of the body region (the doping concentration of P+ region is higher than P region). Hshieh et al. also teach the doped contact region 138 is used to reduce the parasitic resistance (paragraph [0025]).

It would have been obvious to one of ordinary skill in the art at the time of invention was made to combine the inventions of Omura et al. and Hshieh et al. and use the doped contact

region taught by Hshieh et al., because the parasitic resistance can be reduced as taught by Hshieh et al.

25. **Claims 16-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Omura et al. as applied to claim 15 above as can be understood since claims 15-18 have been rejected under 35 U.S.C. 112.

Omura et al. teach, regarding to **claims 16-17**, the doping concentration (Fig. 15B), the drift region (12), the drain region (11), the body region (13), and regarding to **claim 18**, the gate-field plate insulator (18), and the filed plate insulator (16).

Omura et al. do not teach, regarding to **claim 16**, wherein the doping concentration in the part of the drift region adjacent to the drain region is at least 50 times greater than the doping concentration in the part of the drift region adjacent to the body region, regarding to **claim 17**, the doping concentration in the part of the drift region adjacent to the drain region is at least 100 times greater than the doping concentration in the part of the drift region adjacent to the body region, and regarding to **claim 18**, the gate-field plate insulator has a thickness that is greater than or equal to a thickness of the field plate insulator.

Parameters such as the doping concentration and the thicknesses of the gate-field plate insulator and the filed plate insulator in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance, e.g. ON resistance and switching speed as disclosed by Omura et al. in paragraph [0003], or the breakdown voltage and the threshold voltage in paragraph [0065]. Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to

incorporate the doping concentration and the thicknesses of the gate-field plate insulator and the filed plate insulator within the range as claimed in order to achieve desired device performance.

***Response to Arguments***

26. Applicant's amendments, filed 01/29/2008 and 08/29/2008, overcome the objections to the drawings, the title, the specification, and claims 1-10 and 12-14, and the rejections to claims 7-9 and 12 under 35 U.S.C. 112. The objections to the drawings, the title, the specification, and claims 1-10 and 12-14, and the rejections to claims 7-9 and 12 under 35 U.S.C. 112 have been withdrawn. The objection to claim 11 still stands because Applicant does not respond to this objection.

27. Applicant's arguments filed 01/29/2008 and 08/29/2008 have been fully considered but they are not persuasive.

28. On pages 9-10 of Applicant's Response, Applicant argues that Omura simply teach that the impurity concentration of drift layer 12 increases toward the substrate 11. See, e.g., Figure 2 and Paragraph 0053 and the cited portions of Omura do not provide any indication regarding the level of impurity concentration in drift layer 12 near well layer 13 relative to the level of impurity concentration in drift layer 12 near substrate 11, let alone teach that the doping concentration in the drift region has a steeply graded concentration gradient as in the claimed invention.

29. The Examiner respectfully disagrees with Applicant's argument, because firstly Applicant does not define "steeply", which is a relative term, in the original disclosure. The limitation "steeply" is only disclosed in 4$^{th}$ paragraph of page 3 and is not defined. Secondly, the

levels of impurity concentration in the drift region in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance. This is well accepted in the semiconductor industry. Omura already teaches that the increase of the level of impurity concentration in the drift region toward the substrate is important to reduce the ON voltage (paragraph [0054]). Omura also teaches various embodiments to achieve the increase of the level of impurity concentration (Fig. 16 A-C). Omura does not teach the actual levels because the actual levels are in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device performance. The actual levels of impurity concentrations has to be determined through routine experimentation and optimization determined by the ON voltage required by the specific application and also the trade-off between the speed and the breakdown voltage (paragraph [0006, 0027, 0054]).

30. On page 10 of Applicant's Response, Applicant argues that the cited portions of the Omura reference further fail to correspond to aspects of the claimed invention directed to the thickness of the gate-field plate insulator being greater than or equal to the thickness of the field plate insulator. In contrast, Omura teaches that the insulator between buried electrode 19 and gate electrode 17 (i.e., second insulating film 18) has a thickness between 400 to 450A, whereas the insulator for buried electrode 17 has a thickness of 3000A. See, e.g., Figures 7-14A and Paragraphs 0037-0041. Thus, the insulator between buried electrode 19 and gate electrode 17 is substantially thinner than the insulator for buried electrode 17.

31. The Examiner respectfully disagrees with Applicant's argument, because the thicknesses of the gate-field plate insulator and the filed plate insulator are subject to routine experimentation

and optimization to achieve the desired device performance. This is well understood in the semiconductor industry and is well supported in Omura reference. Omura reference teaches the gate-field plate insulator 18 is determined by the threshold voltage, and the thickness of the filed plate insulator 16 is determined by the breakdown voltage (paragraph [0031]). The actual thickness of the gate-field plate insulator 18 and the filed plate insulator 16 are determined by the trade-off between the breakdown voltage and the speed associated with a specific application (paragraph [0027]). Omura reference proposes some thicknesses, but these thicknesses are examples (paragraph [0031]). The actual thicknesses still has to be determined by the routine experimentation and optimization to achieve the desired device performance, e.g. the speed (e.g. ON resistance) and the breakdown voltage.

32. In response to Applicant's argument on pages 10-11 that the Office Action cites to the Abstract of the Miyano reference without relying on the underlying document or providing an English translation of that document, the Examiner provides the English translation of Miyano reference in this Office Action. The § 103(a) rejection of claim 3 is still maintained as the underlying document is consistent with the Abstract. This action is made final due to Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action.

33. On page 11 of Applicant's Response, Applicant argues that Office Action has not provided any evidence that replacing Omura's gate electrode 19 with Miyano's gate electrode 3 would reduce the capacitance between the electrode and substrate 11 in Omura's device. As such, the Office Action fails to provide a sufficient reason why the skilled artisan would combine the references as required.

34. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Miyano et al. teach the shape of the gate reduces the capacitance between the gate and the drain, and a high speed operation can be performed (Abstract).

35. On page 11-12 of Applicant's Response, Applicant argues that Omura's source electrode 21 does not extend through source layer 14 to well layer 13 as does the additional trench filled with conductive material of the claimed invention.

36. The Examiner respectfully disagrees with Applicant's argument, because Omura's source electrode 21 does extend through source layer 14 to well layer 13 in the horizontal direction (Fig. 4 of Omura). Omura's reference reads on claim 7.

***Conclusion***

37. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). Applicant introduces new limitations into the independent claim 1 and also introduces new claims 15-18.

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsin-Yi (Steven) Hsieh whose telephone number is 571-270-3043. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811

/H. H./
Examiner, Art Unit 2811
12/23/2008